ABSTRACT

A method of fast random access management of a DRAM-type memory, including the steps of: dividing the memory into memory banks accessible independently in read and write mode; identifying the address of the bank concerned by a current request; comparing the address of the bank concerned by a current request with the addresses of the N-1 banks previously required, N being an integral number of cycles necessary to the executing of a request; and if the address of the bank concerned by a current request is equal to the address of a bank corresponding to one of the N-1 previous requests, suspending and memorizing the current request until the previous request involving the same bank is executed, otherwise, executing it.